EXHIBIT 7

QUANTEL LIMITED

DLS 6000 SYSTEM

SERVICE MANUAL

SECTION 2 SYSTEM CONFIGURATION

2.1 Brief Description

See Figure 2.1. The system comprises:

(a) DLS 6000 Main Frame

The main electronics frame which houses the framestores, all the video processing circuitry and the system control electronics.

(b) Winchester Discs

Up to eight industry standard Winchester discs, which connect to the main electronics rack by means of BUS and RADIAL cables as shown in Figure 4.3.

(c) Control Panel

One or two control panel stations, which communicate with the main electronics rack by means of the standard RS422 interface. If only one station is used, it may be switched to control the editorial facilities or on-air outputs at any particular time. If two stations are connected, then one may control the on air outputs and the other editorial facilities concurrently; a lock-out mechanism prevents both stations trying to control the same function at any one time. Each control panel station comprises a control panel processor (housing power supply unit and a micro processor to provide local control) and a selection of panels.

(d) Line Printer

If desired, an industry standard line printer may be connected to the main electronics rack to provide printouts of picture titles, stacks, etc.

(e) LSI-11 Computer

Early systems were supplied with an external LSI-11 computer, which was connected between the control panel stations and the main electronics rack.

In later systems, the functions of this computer are performed by the cards Computer 1 and Computer 2 housed in the main electronics frame.

(f) If desired, an industry standard video recorder may be connected to the Main Frame for picture archives.

2.2 Control Panel Types

The type A panel is a replay only panel, allowing individual pictures or pre-recorded stacks to be accessed for the on air outputs. The type B panel is a record/replay panel, switchable to control the on air outputs or editorial facilities. The type C panel is an effects panel, which is used in conjunction with a type B panel to programme size/position change, border, matte, crop, fade, etc., effects in the editorial mode.

The keyboard is used for typing in titles, and to control all the title sorting functions.

SECTION 2 PRINCIPLES OF OPERATION

2.1 System Description

A broad block diagram of a fully configured 6000 system is shown in Figure 2.1.

Figure 2.2 shows the control and video paths in more detail and should be used in reference to the following section.

Incoming video is routed to the input processor where timing information is extracted from the syncs and burst, and the video is digitised. The data passes through the key/encoder, where certain areas of the picture may be replaced by $\overline{\text{KEY}}$ in accordance with the key input signal; this allows captions to be recorded which are intended to be superimposed on other pictures. The data is then written into the editorial store using addresses generated by the encoded address system. The output processor extracts timing information from the syncs and burst of the reference video input, which is passed via the cursor card to the encoded address system, causing data to be read out of the editiorial store. This then passes through the tape interface (or its bypass card) where the cursor (crosswires) is superimposed as required by the cursor card, and then through the tape buffer (or its bypass card) to the output processor. Here it is converted back to analogue form, syncs and burst added, and the composite video signal thus obtained passes to the preview (PVW) output.

Data frozen in the editorial store may be recorded onto a Winchester disc. In this case, timing information from the appropriate disc passes through its associated SMD interface card(s), the disc sequencer, disc data buffer and clock interpolator and via the system bus to the encoded store address system. It is used to read data out of the editorial store, but the tape interface now passes this data to the system bus. It then passes through the disc data buffer (where it is serialised), and the appropriate SMD interface card to the selected disc.

When it is required to recall a picture from a disc, the disc timing information follows the same path as described above from disc onto the system bus. In this case, however, the clock interpolator may reduce the number of clocks passed so as to alter the picture size as required. The data passes through the appropriate SMD interface card to the disc data buffer, where it is deserialised. In the decoder, the signal is split into its luminance and chrominance components; these are filtered as necessary by the filter, whose outputs are enabled onto the system bus. If the picture is required in the editorial store, the data is taken from the system bus by the key/encoder, which recombines luminance and chrominance to give encoded signal suitable for the editorial store. The encoded address system takes the timing information from the system bus and uses it to generate the necessary address for the editorial store. If, however, the picture is required in one of the main (decoded) stores, the data is written directly from the system bus into the appropriate one in decoded form, the decoded address system generating the necessary address from the disc timing information present on the system bus.

In either of these cases, the cursor card may be active in generating a CROP signal for the appropriate store to inhibit certain areas of the picture from being written. This allows the edges of pictures to be cropped off, or the selection of just part of the recorded image. The cursor card also detects $\overline{\text{KEY}}$ areas of the recorded data and prevents the writing of these into the stores (using the crop signals), thus allowing captions to be superimposed on pictures.

The outputs of the decoded stores are encoded on the decoded output processors, and each of these supplies its encoded output to both of the combiners. Each combiner then selects one of these, or a weighted combination of each during a fade, and passes the resulting signals to its associated decoded output processor. It it there converted to an analogue signal, syncs and burst added, and the composite video signal thus obtained passes to the main output. It should be noted, therefore, that the signal at, say, the video I output may have originated at store I or II, and may thus have been encoded on decoded output processor I or II.

If it is desired to write a border or matte into any of the stores, the data and timing pulses originate at the key/encoder and are enabled onto the system bus. For the editorial store, the key/encoder itself uses the data to form an encoded signal which is written into the store under the control of the encoded address system. For either of the main stores, the data is written directly from the system bus into the appropriate one in decoded form, under the control of the decoded address system. For any of the stores, the border data consists of the actual luminance and chrominance values giving the desired border, but the matte data is the code specifying a $\overline{\text{KEY}}$ area. At the output of the editorial store, this code is detected on the tape interface (or its bypass card) and replaced by a level giving 5% setup. At the output of the decoded stores, however, the code is detected on the decoded output processors and passes to both combiners as a KEY signal. Each combiner can then put appropriate matte levels in the $\overline{\text{KEY}}$ areas, and combine its two input keys in the same way as it is combining its two input data streams. Thus a combined KEY signal is generated to accompany each of the main outputs, which at all times represents the picture area of its associated video output.

For bulk storage, pictures may be transferred from disc and recorded onto normal video tape in digital format (dump) and later transferred back into disc (load). The same path may be used for transferring pictures between equipments. During dump or load the disc timing signals are supplied to the system bus in the manner already described for other disc accesses. During a dump, the data is enabled directly onto the system bus after deserialising by the disc data buffer. It is loaded into the tape buffer under

the control of the tape interface, through which it passes to be serialised and formatted in a manner suitable for passing to the output processor and hence to the preview output. During a load, the data passes directly from the input processor to the tape interface, where it is deserialised and passes to the tape buffer. It is then enabled onto the system bus, and passes to the disc via the disc data buffer in the normal manner. In both dump and load, the tape buffer provides the storage necessary to buffer the data as its speed of progress changes between disc and tape speeds.

The various modes of operation just described are selected and controlled by a computer, which may consist of two internal computer cards or an external computer. In either case, the computer issues its commands to the various parts of the system via the system bus. Several of the data transfers which have been described also take place over the system bus. Thus it should be appreciated that this bus serves two distinct purposes; having issued commands which initiate such a data transfer, the computer must then relinquish the bus until such time as the transfer is complete. The computer needs to store certain information on the disc to enable it to perform later operations correctly (disc directory, titles, stacks of picture numbers, etc). A route is thus made available from computer to disc via a buffer on the disc data buffer, by means of which such information transfers are handled.

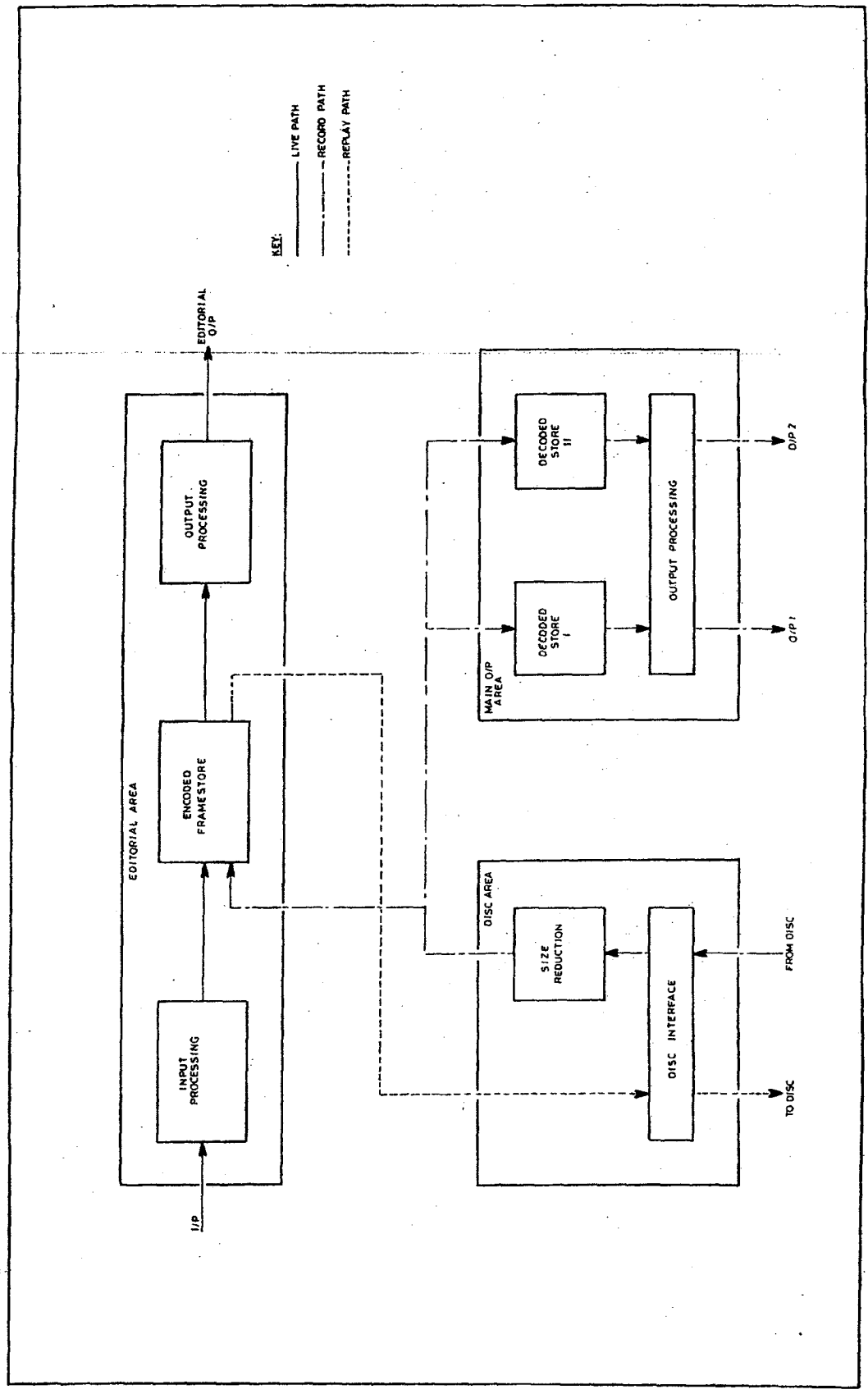
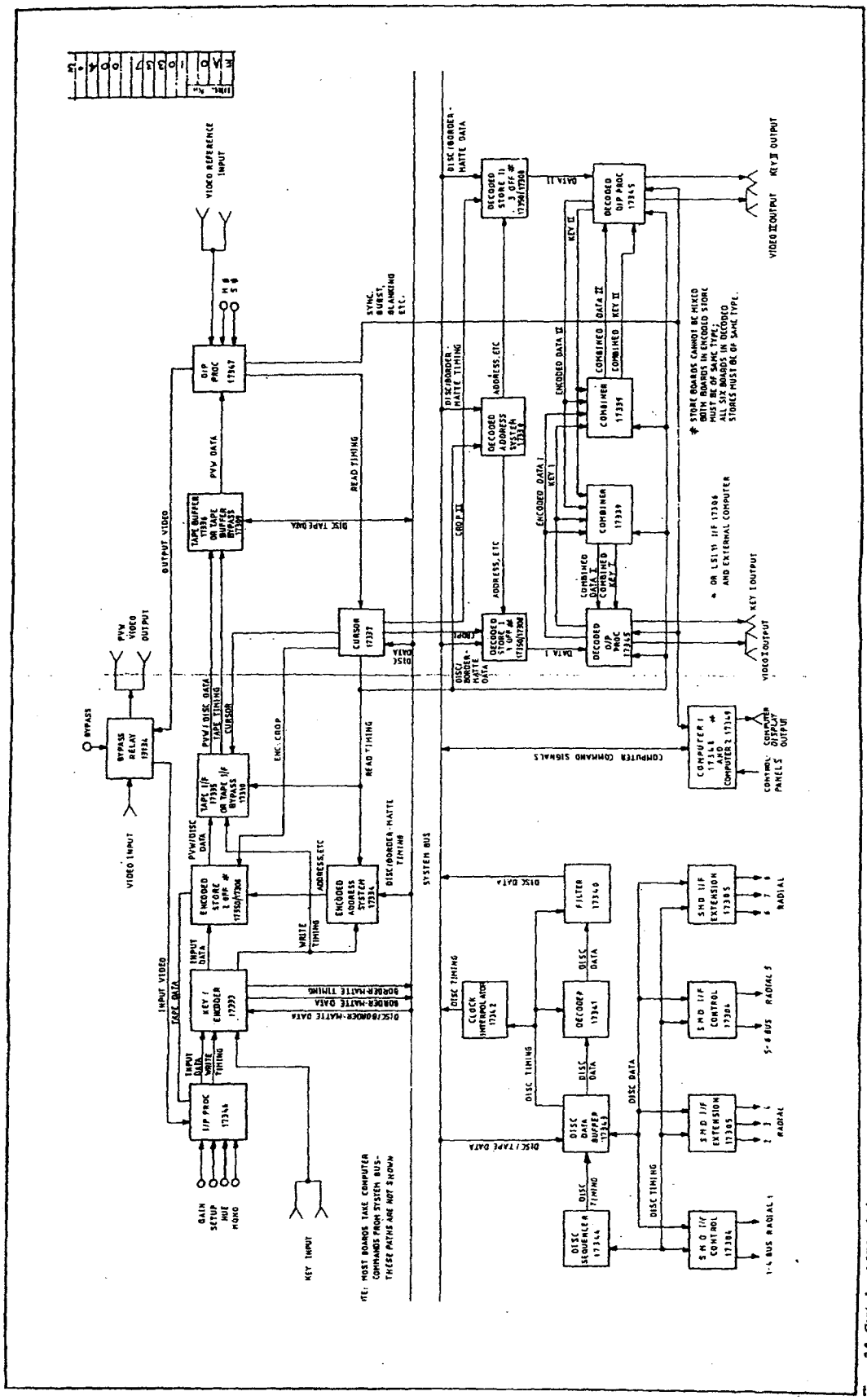


Figure 2.1 DLS 6000 Block Diagram

SERVICE — MANUAL



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DISC SEQUENCER CARD

17344

1. Circuit Description

This card uses an AM2910 bit slice sequencing element. This provides the addressing for a 56-bit wide micro code word which is stored in seven 28L22 PROMs The outputs of the PROMs are registered before use, providing signals S0 through S55.

S0 through S7 are fed back to the 2910 and are used to supply any jump address which may be required by a sequencer instruction. S8 through S11 are also fed back to the 2910 and constitute a 4-bit instruction to the sequencer. The gate GH, which is in series with the sequencer instruction word, gives the ability to force the instruction code to zero which is the 'jump to start' code. The sequencer is forced to the 'start' state by any of the following:

(a) Absence of 1MHz clock, causing monostable DB to time out and clear the two halves of BG.

(b) A 'panic' clear command issued by the control computer, usually invoked by a time out condition occuring due to a sequencer hang caused by a disc error. The control computer issues a 'panic' clear by setting the CSR code to fifteen and putting TX/RX low. This is detected by CA which clears BG.

(c) An end of sequencer program signalled by setting S25 which clears the first half of BG, which clears the second half on the next clock cycle.

S12 through S16 drive FF, FE, FD, FC and FB which form a one of 32 data selector. This provides 32 condition code inputs to the AM2910.

S17 and S18 are clock and clear to EF and EE. These are used to count lines, a count of 25 being detected by bit zero of DF which is fed to the sequencer as a condition code. Bit one of DF is unused.

S19 and S20 are clock and clear to ED. Only the Qa output is used at the moment to flag an error condition to the control computer.

S21 and S22 are clock and clear to EC. In auto-head mode EC selects head numbers, with prom DC acting as a comparator. At present this mode is not invoked and DC is replaced with a link between pins five and twelve of the PROM socket.

S23, S35, S36 and S37 are four signals used to strobe the appropriate information onto the disc bus cable.

S24 enables the cylinder number data onto the disc bus cable.

S27 enables the command word to the disc onto the bus cable, S26 through S34 being the actual command word.

S40 through S47 and S53 are control signals to the disc data buffer card and are explained in that card's circuit description.

S54 is a disc-rate line sync output and S55 a disc field reset.

AA, AB and AC buffer the control bus. BA detects CSR code = one indicating a disc access is required. CB decodes the top four bits of the control word. If the value of these bits is zero, the data on the first ten lines of the control bus is interpreted as a cylinder number and is clocked into AE and BH. If the value of the top four bits is two, the data and the other twelve lines of the control bus is interpreted as a command to the disc sequencer and is clocked into DD and CC. Additonally BG pin six is clocked to a zero pulling REQB low, signalling a 'bus busy' state. This remains low until an end of command is flagged by the sequencer which clears BG. BC holds the disc status word which can be read by the control computer.

Bits zero through three of the command word hold the disc head number and with bit four low, the head number is tri-stated onto the disc bus with DE. Bits five, six and seven of the command word hold the drive number. Five and six are a one of four select to the disc bus cable. BE decodes all three drive number lines and feeds the SMD interface cards.

DISC DATA BUFFER CARD

17343

1. Circuit Description

This card provides parallel to serial conversion for writing to the disc, serial to parallel conversion for reading from the disc and formats disc data under control of the disc sequencer. In addition to these functions, this card has a data buffer which has sufficient capacity to store one complete disc track of data. This is used to give the control computer access to the data stored on the disc and also enables the computer to write data such as directories onto the disc.

The disc controller system runs on a 1MHz clock. This is obtained from a divide by eight counter, IB. The 8MHz clock to this counter can come from one of three sources, selected by AG under control of the sequencer. When a disc transfer is not taking place, the clocks are switched to an on board 8MHz source, HF. During writes to the disc, the servo clock is used as the 8MHz source and during reads from the disc, the disc read clock is used.

Serial data being read from the disc is clocked into BG. The parallel output of this shift register feeds BF which strobes the data at an appropriate time to give de-serialised data at 1M byte per second. The output of BG also feeds DF and DG which act as a sync word detector. When data is written to the disc a sync word is written at the beginning of each track to enable the de-serialiser to lock to the appropriate 'frame' of 8-bits. A second sync word is written at the end of a track in order to check for framing errors. The sync word detector is armed by the sequencer by sending a clear pulse to IC13 which enables DG. When a sync word appears across the parallel output of BG, DG9 goes low which in turn sends IC5 low on the next 8MHz clock cycle. At this time the sync word has been shifted down BG so DG9 will return to its high state. At the next clock cycle IC5 goes high again, disabling the sync detector by clocking IC8 low. Meanwhile IB has been preset with the low pulse from IC5, which has now phased up the byte clock with the serial data stream.

HC, HD and HE count the 1M byte per second clocks and only allow clocks to be output which correspond to valid picture points, totally 767 per line (768 in tape transfer mode).

CG is used to serialise data when writing to the disc. ID is used to generate a load pulse after a positive transition of the byte clock. The eight bits of data are then shifted out with the 8MHz bit clock. Data can be supplied from serveral sources (under control of the sequencer) detailed below.

(a) CF provides a source of all zero which is used to write gaps preceeding the sync word and between the sync word and data on the disc.

(b) CC provides the sync word pattern.

(c) CD picks up the encoded video data from least significant eight bits of the control bus.

(d) CE enables data in the RAM buffer store to be output to the disc.

AA, AB and BC buffer the control bus . CA decodes CSR codes zero, one and seven. GA 9 holds the tape mode bit of the computer status word. This is used to control the picture point counter HC, HD and HE. It is also used to route data from the disc onto the control bus, via BE, in tape mode. With CSR code one selected (disc command word) BA is enabled, which then decodes the top four bits of the control word. If this has a value of two a disc transfer command has been issued and the R/W bit is stored at GA5. In read mode this is low which puts a parameter clear on output shift register CG which reduces the noise pick up on the disc radial cable. GA6 is used to gate the enable of BE so that it is only enabled during disc reads when in tape mode. If the top four bits of the control word have a value of one, 'preset RAM address' command has been issued. This causes IA6 to go low which feeds the load inputs of the RAM address counters DA, DB, DC and DD. It also triggers HA1 which provides a clock for the counters while their load input is low. The address to which the counters need to be preset appears on the lower twelve bits of the control bus.

With CSR code seven selected, the control computer has the ability to read from or write to the data buffer RAM. When reading from the RAM TX/RX goes low and data out of the RAM is enabled onto the eight least significant data lines of the control bus with BB. When the control computer has read a byte it pulses DTX which clocks the RAM address counters to the next address. When writng to the RAM an NDR is generated at IE8. This clocks the data on the eight least significant data lines of the control bus into CB. It also triggers monostables HA9 and IG1. HA enables data to the RAM's while IG pulses the write enable pin of the RAM's. The latter also serves to clock the RAM address counters onto the next address via IF 12.

The sequencer has control of the RAM with signals 'Read RAM', 'Write RAM' and 'Zero RAM Address'. When 'Read RAM' is pulse CE is enabled, routing the RAM output to the data serialiser. This signal also feeds IF2 which clocks the RAM address counters. When 'Write RAM' is pulse BE is enabled routing data from the disc to the RAM. This signal also pulses the write enable line on the RAM and clocks the RAM address counters via IF10. 'Zero RAM Add' simply clears the RAM address counters.

EC6 goes high when an address count of 19200 is reached. This signal is fed back to the sequencer flagging that a complete track of data has been transferred from or to the RAM. This number is made identical to the number of picture points stored on a track in video mode. This allows all tracks to be written or read as data or video which gives the control computer the ability to add title information onto the end of a video track.

CLOCK INTERPOLATOR CARD

17342

1. Circuit Description

The basic function of this card is to take in the clock signals from the disc and operate them so as to omit some of the clocks on a regular and controlled basis, in order to change the size of the picture as it is being taken from the disc into a framestore. The picture size is determined by the number of clocks remaining; for example, if one clock in three is omitted, then 2/3 remain, and so the picture will be 2/3 of full size. The card operates separately on disc picture point clocks (DPPCK) and disc line clocks DLCK, so that the picture aspect ratio may be changed, using similar circuit configurations. The outputs are called interpolated disc picture point and line clocks (IDPPCK) and (IDLCK).

A block diagram of the basic circuit configuration is shown in Figure 1.

The counter and accumulator both start at zero. The counter increments on each input clock. The accumulator is clocked only when an input clock is passes to the output (i.e. as an interpolated clock), and causes a number representing the required picture size (called the reduction ratio) to be added into the total already present in the accumulator. An output clock is derived only when the comparator output is true, that is when the whole number part of the accumulator is equal to the counter.

For example, suppose a picture 2/3 of full size is required. The reduction ratio is thus 3:2 or 1.5:1. Initially the counter and accumulator are both zero, so the comparator output is true; the first input clock passes to the output and the counter and accumulator output 1.5. The comparator output is still true (only the whole part of the accumulator output is used by the comparator); the second input clock also passes to the output and the counter and accumulator are both clocked. Now the counter output is two and the accumulator output three. The comparator output is thus false; the first input clock does not get through to the output, and so only the counter is clocked. Now the counter output and accumulator output are both three, and the cycle repeats as from zero.

There have been two output clocks for the three input clocks, as required.

Note that the fractional output of the accumulator at each step represents the error between the position of the data sample required and that which is available. It can be used by the filter card to calculate an output data value by interpolation.

X	X	X	X	X	X	Input Clocks
X	X		X	X		Interpolated Clocks
0	0.5		0	0.5		Group Delay
X		X	X		X	Required Output Data Position

The horizontal section repeats its operation each line, initiated by DLCK and interpolates DPPCK to give IDPPCK. The reduction ratio is loaded into BH and CH (whole and fractional respectively) from the computer bus by address decoder AA. BE, CE DE form the picture point counter; BF CF, DF form the comparator, etc.

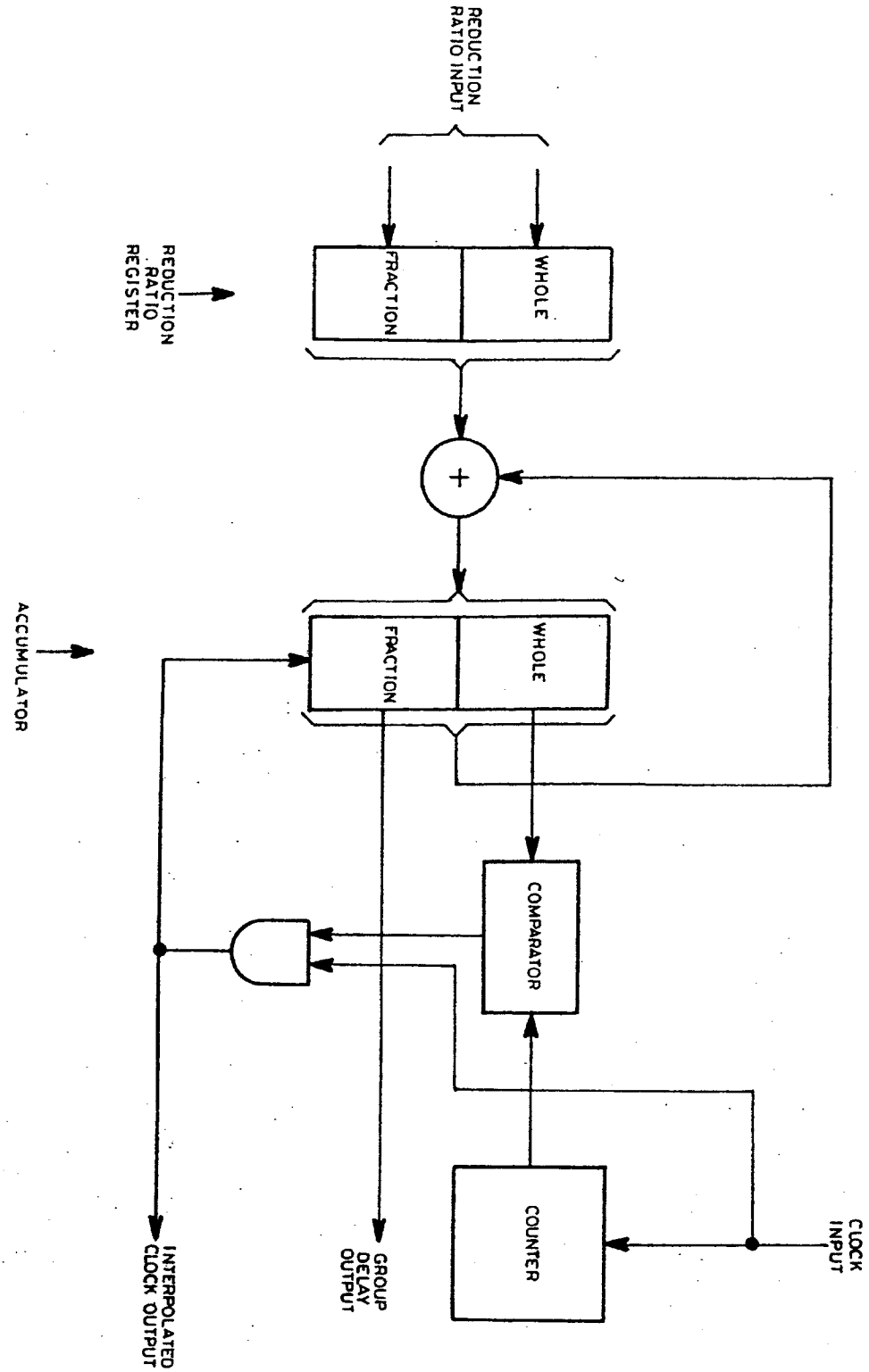
The most significant three bits of the accumulator fractional output leave the card via AD as horizontal group delay (HGD).

The vertical section repeats its operation each field or frame (as indicated by the computer at AI pin nine) according to the type of picture stored on the disc. It is initiated by disc clear (DCL) and interpolates DLCK to give IDLCK. The three most significant bits of the accumulator fractional output leave the card via AK as vertical group delay (VGD). The most signficant of these may be set high initally (by presenting EB pin nine) for the second field of a field mode picture so that the filter generates the second field data from the recorded (first) field by interpolation.

The circuiting comprising GD and parts of GE, GB, GG, FE and EF simply delays each IDLCK by a preset number of IDPPCKs to generate a delay disc line clock (DDLCK); this delay compensates for the number of pipeline latches through which the data passes between the disc and the framestore and is set for PAL or NTSC by LK1.

The card also outputs a disc field (DFB) which is either IDLCK divided by two (at GE pin five) in frame mode, or computer generated (at AI pin six) in field mode. The computer selects which of these is required by means of selector GF. The computer also determines whether the interpolated clocks or the input clocks direct are used at the card output by means of control signals in the status word loaded to AI, which control the tri-state inputs of buffers AF. The former are used for all disc read operations, and the latter for all disc write operations.

Note that for NTSC operation, PROM's EA and GA are not fitted; GA pin fourteen is wired permanently low.



17342 Figure 1 Clock Interpolator Card Block Diagram

DLS 6000-17342-Issue A-11/82

DECODER CARD

17341

1. Circuit Description

The purpose of this card is to take video data as it comes from the disc and separates it into luminance and (demodulated) chrominance components. It should be appreciated that the card works at disc speed; therefore references to things such as 'one line delay' do not mean a real time delay of one line, but a delay such that input and output values are sampled from consecutive lines.

The principles of operation are best understood by reference to the simplified block diagram.

In the band pass filter, an average between two data values separated by four picture points (A and C) is calculated, and then the data value midway between the two (B) is subtracted from the result. Subcarrier components are in phase between A and C, but 180°C different at B. The result is that at D, the d.c. components are totally cancelled, whilst the subcarrier components are present at full amplitude; at other frequencies, partial cancellation will have occured. Thus we have a band pass filter (with gradual cut off), centred around the subcarrier. Only frequency components within this pass band will be used in the subsequent vertical comb filter for separating chrominance.

Registers BA, CA, DA and EA provide the four picture point of delay, point A being the input to BA and point C being the output of EA. The average between A and C is clocked into register CB; therefore the intermediate point B is taken not from the output of CA but from the output of DA, so that there is a corresponding picture point of delay. DA and EA are both inverting registers. The output of DA is therefore bit-inverted (as is required for DB and EB to act as a subtractor), whilst the output of EA is back to normal polarity. The output of the subtractor is clocked into register FB to provide the output D. It should be noted that data at D has undergone four clocks of delay, whilst that at C has undergone four clocks of delay; subcarrier components at these points are therefore 180° out of phase with each other.

In the combiner filter, an average between two data values separated by two lines (D and F) is calculated and the output is subtracted from the data value midway between the two (E). As subcarrier components alternate in phase from one line to the next, at the output of G these will present unattenuated, whilst other components will have been cancelled. It remains only to demodulate the signal at G to obtain the chrominance output.

In principle, the lumianance output is obtained by subtracting the signal at G from the original signal. However, the signal at G has undergone a one line delay from point D; we therefore need a corresponding one line delay from C to H. As was noted earlier the subcarrier components at points C and D are 180° out of phase with each other, and therefore effective subcarrier removal is obtained by adding the signal at G to that at H.

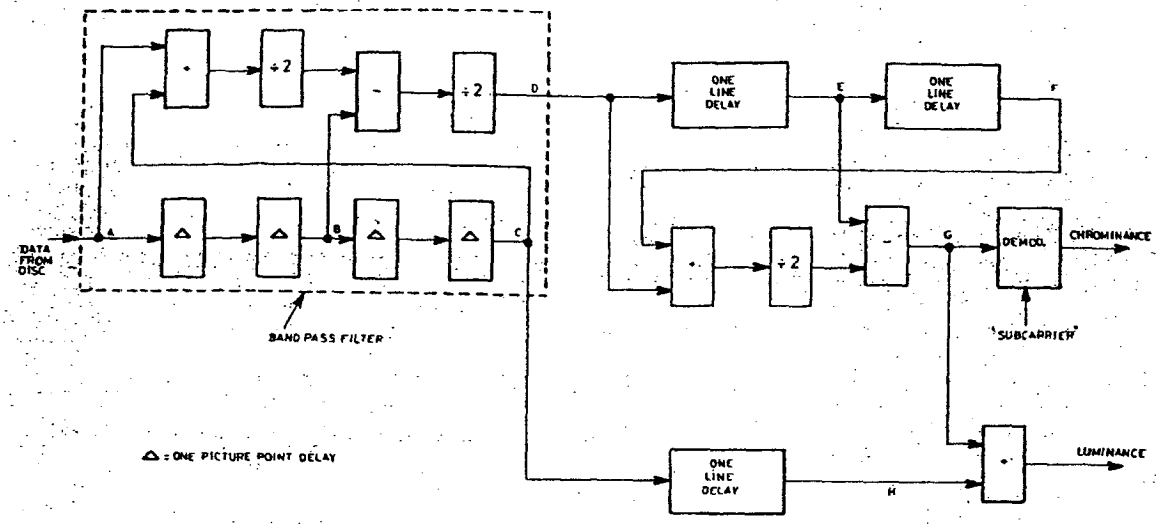
The above description has assumed a field mode picture, that is field one followed by field two as for normal video. In frame mode, the picture is de-interleaved, that is consecutive lines are from alternate fields. Hence, to decode in the same fashion as described, each of the one line delays must be replaced by a two line delay, so that consecutive lines of the same field are used in the manipulation as before.

We are now in a position to relate this to the circuit diagram. Counters ID, 1E and IF are reset to zero each line counts picture points along the line, so generating addresses for CH, DH, EH, FH, AH, and BH, which each provide one line of delay. This is accomplished under the control of signals from ROM IB driven by counter IA, such that for each picture point the old data value (from one line ago) is clocked from the RAM into the subsequent register during the first part of the cycle, and the new data value is written from the preceeding register into the RAM during the later part of the cycle. The data selectors EF, FF, GF, HF, CF and DF switch between field and frame modes as selected by the computer via address decoder AA and flip-flop AB. Thus, in field mode, CH is the delay between points D and E (of the block diagram), DH is that between E and F, and BH is that between C and H. In frame mode, CH and DH are between D and E, EH and FH are between E and F, and BH and AH are between C and H. Data between points D and F is averaged in adder GC, GD and part of GE, and subtracted from that at point E in subtractor GB, FC, FD and part of FE. The demodulator comprises DC, EC, CD and BD using disc rate 'subcarrier' made by dividing disc picture point clock by four in HA. The phase of this 'subcarrier' is alternated line by line (for field mode) or after each two lines (for frame mode) by the appropriate signal from IH as selected by HH. The addition of signals at points G and H is accomplished by adder DE, CE, and BE, whose output is limited to the range zero to 255 by BF and BG to provide the luminance output.

The combiner filter works effectively only if there is no substantial difference in data over the two lines of interest, that is between D and F. To avoid any possibility of significant residual subcarrier effects, it is possible to modify the operation of the decoder if this condition is not satisfied. To this end, the difference between data at D and F is found by subtractor HE, HD, HC and part of GE. This is used to address PROM HB whose output is high unless the diffenece exceeds a predetermined level, when the selectors ED and DD will no longer pass the sub carrier component at point G but will pass the data from point E. In this case, the luminance output will consist of the difference between the card input signal and the output of the band pass filter, that is

with all components in the wide notch centred on subcarrier removed. This ensures that no chrominance is present on the luminance output, at the expense of having removed some of the luminance components in the chrominance passband.

The signal level consisting of all bits high (i.e. 255) at the card input represents the area of picture which is not required, i.e. KEY. This needs to be changed so that it is represented by all bits low (zero) at the card output. The 255 level is detected in EE, which forces the limiter BG, BF to operate at its low limit (i.e. to set its output low) via diode D2. The latched key output on A23 is not used.



17341, Figure 1 Decoder Card Block Diagram

FILTER CARD

17340

1. Circuit Description

The function of this card is to filter the decoded video data in the horizontal and vertical axes as it passes from the disc to a framestore, using algorithms (i.e. sets of coefficients) suitable for the size chosen for the picture. The horizontal filtering is accomplished in multiplier-accumulator EF using data values stored in RAM CH and coefficients stored in RAM CE. The vertical filtering is accomplished in a similar circuit, the multiplier-accumulator EC operating on data values stored in RAMs HH, HG, HF and HE using the coefficents stored in RAM CD.

Before each picture transfer, the computer loads sets of suitable coefficients into the two coefficient RAMs via the bus (D0-D15), using address decoder AA and monostables BA.

Each disc picture point clock (D.P.P.CK.) interval is split into eight sections, by counting the (disc) bit clock signal in FE; its outputs provide three of the address bits to both coefficient RAMs. A similar sequence of address is required to access consecutive locations in the luminance data RAM CH. However, to avoid having to rewrite the whole of this RAM for each picture point, (that is to move the data to adjacent locations in shift register style), the addresses are adjusted by one on each consecutive picture point, in a cycle that repeats each seven picture points (as the horizontal filter operates over a seven picture point data block). This adjustment is accomplished by ROM BF which has inputs the straight count zero to seven (FA outputs) and a cycle of seven picture point count (AG output). Hence the addresses of CH will follow this pattern:

1st picture point, 0 1 2 3 4 5 6, write new data to 0

2nd picture point, 1 2 3 4 5 6 0, write new data to 1

3rd picture point, 2 3 4 5 6 0 1, write new data to 2

etc., down to

7th picture point, 6 0 1 2 3 4 5, write new data to 6

and then repeat.

In each case, as is shown, the incoming data is written into the location which was used first, i.e. the one which previously held a data value seven picture points before the incoming one, and is thus no longer needed. BF also supplies (via DF) a write pulse for CH at the appropriate time. Thus in each of the eight sections within the D.P.P.CK. interval, a coefficient and data value are presented to EF, which multiplies the two together and adds the product into its internal accumulator. However, BF produces a signal to drive pin twenty of EF low once per D.P.P.CK., so that the first product calculated is loaded straight into the accumulator, rather than being added to what remains there from the previous D.P.P.CK. Different sets of coefficients may be selected for each picture point according to the degree of interpolation required, which is indicated by the horizontal group delay (H.G.D.).

In certain circumstances, the use of negative coefficients is desirable. Here pin sixteen of CE will be high. However, because of the internal operation of EF in its subtract mode (i.e. the previous contents of the accumulator are subtracted from the current product), the signal required to drive EF pin ninteen is one which indicates when the current coefficient differs in sign from the previous one. Such a signal is generated in GC and EE.

The output from EF is limited to the range zero to 255 by EG and DG, which are driven by overflow and underflow outputs from EF, and then clocked into GD by D.P.P.CK. Thus the luminance data values here have been filtered in the horizontal axis.

This data then passes through the vertical filter which works in a similar fashion to the horizontal filter. However, instead of presenting adjacent data values to EC, it is necessary to present picture points from consecutive lines. Hence there are four line stores HE, HF, HG and HH, which together with the incoming data at the output of GD allow for filtering over five lines. The counters HB, HC and HD simply count D.P.P.CK.s along each line to address the lines store RAMs. The correct line for use during any particular section of the D.P.P.CK. interval is selected by ROM GA, whose inputs are the straight count zero to seven (FA outputs) and a cycle of four line count (EB outputs). Hence the selects to the line stores will follow this pattern:

1st line, each picture point 1 2 3 4 GD, write new data to 1

2nd line, each picture point 2 3 4 1 GD, write new data to 2

3rd line, each picture point 3 4 1 2 GD, write new data to 3

4th line, each picture point 4 1 2 3 GD, write new data to 4

and then repeat.

The required set of coefficients is selected by the vertical group delay (V.G.D.), and the rest of the circuit operates as already described.

Filtered luminance is finally clocked into AC, whose outputs are enabled onto the system bus during disc picture read operations by the appropriate bits in the status word, which has been loaded into CA by the computer.

The chrominance data is not filtered, but passes through this card in order that it may suffer the same delay (both horizontally and vertically) as the luminance. BG is clocked at the appropriate time during each D.P.P.CK. interval by a signal from ROM BF, that is whilst the address is taking place. BD and BC which are selected alternately, provide two lines of vertical delay. Alternate chrominance data samples are clocked into AB and BB by the half of CB which toggles on D.P.P.CK.s; hence all B-Y samples pass through one and all R-Y samples pass through the other. They are enabled onto the system bus alternately during disc picture read operations by the other half of CB, which toggles on L.D.P.P.CK.s. This is because not all of the output samples will be taken off the bus (for picture size changing operations), and it is necessary to ensure that alternate points which are used are B-Y and R-Y samples.

STORE CARD

MKI 17350

MKII 17308

1. Circuit Description

Whilst either type of card may be used (the two being very similar), a link on the Address System card needs to be set according to the type used. Thus card types cannot be mixed; both cards in the editorial store must be the same, and all six cards in the decoded stores must be the same. The MKI card uses 32k RAM, whereas the MKII card uses partial 64k RAM.

Each store card contains six stripes, a stripe consisting of eight RAMs (one for each data bit). Input data is clocked into registers IC11 and IC12 of the appropriate stripe by one of the Input Enable signals. These are timed by the Input Enable on AB38, and distributed amongst the stripes by AC under the control of Input Card Select on A36 and Write Addresses WA0, 1 and 2 on B36, A37 and B37. Any particular Input Enable may be inhibited, however, by the CROP signal on AB39, to prevent particular parts of a picture being written. The signal INPUT SELECT changes state just before a write store cycle takes place; data from IC11 and IC12 is thus transferred to the main memory IC1-8 whilst new data is being clocked into the input registers. As the RAMs of all stripes are cycled together, it is necessary to ensure that data written only on those stripes where valid data is present in the input registers. This is achieved by the circuitry consisting of IC13, IC14 and IC15, which inhibits RAS from reaching any stripe which has not received an Input Enable pulse between the last two changes of state of the Input select.

During read cycles, data is transferred from the RAMs of all stripes into the output latches IC9 and IC10 by Output Strobe on AB26. Output select then changes state so that more data may be transferred from the RAMs whilst the original data is being used at the card output. The output registers of the required stripe are enabled onto the output bus by one of the OUTPUT ENABLE signals. These are distributed amongst the stripes by AF, under the control of Output Card Select on A24 and Read Addresses RA0, 1 and 2 on B24, A25 and B25; OUTPUT ENABLE on AB22 is held permanentlly low.

The 32k RAMs used on the MKI card have two RAS inputs, and so the RAS signal on AB13 is passed to the appropriate one (RAS1 or RAS2) according to the sense of the address line A7 on AB21. However, the partial 64k RAMs used on the MKII card have only one RAS input, and an extra address input to which A7 is applied.

It should be noted that the two inputs Picture Enable on AB32 and Caption Enable on AB33 are held permanently high, and so IC16 passes RAS to all RAMs in the stripe all the time.

KEY/ENCODER CARD

17333

1. Circuit Description

The circuitry on this card can be divided into three main areas:-

(a) Write timing signal generation, including the write bit picker;

(b) Video data path, including the input key circuit and the encoder; and

(c) Border/matte generator.

(a) Write Timing

The signal CLEAR WRITE DRIVE (CLWD) entering the card at A15 triggers BF to provide a vertical reset pulse of suitable length, CLEAR WRITE (CLW), for the rest of the machine at B15. As CLW is locked to the vertical component of the video input to the machine, it appears to alternate in position by half a line on alternate fields relative to the horizontal component. Thus sampling Write Picture Gate (WPG) which enters the card on A16 and is locked to the horizontal component of the video input, with CLW in BG generates Write Field Bit (WFB) to indicate which field is present at the input, and which leaves the card on B16. The counter CH, EH, AH is cleared by each field by CLW and clocked by Write Line Reset (WLR) entering on A19; it counts lines down the field. The PROM DH, addresses by the counter outputs, gives two vertical blanking signals, one of which gates WLR to give Write Line Clock (WLCK) on B17. Mono clock gate (MCKG) form A14 or the horizontal blanking signal from the bit picker (see later) is selected under the control of MONO from A12 in CG for adding to the other vertical blanking signal to give Write Blanking (WB) at B14. The four times subcarrier frequency signal (W4FSC) at A18 is gated by WB to give Write Picture Point Clock (WPPCK) at B17. Write Colour Phase Ident (WCPI) at A20, a signal indicating the sense of the write subcarrier line by line, is passed unchanged or inverted according to the level of FLIP on AH to BE pin six; FLIP is generated on the cursor card to control the phase of operation of the write bit picker. The signal at BE pin six is sampled on the rising edge of WFB in FH to give two WRITE COLOUR FRAME IDENT (WCFI) (1) and (2) signals at B11 and B12, which are thus high on one type of write frame and low on the other.

The bit picker is that piece of circuitry which determines exactly which of the clocks is used for the first picture point in any line, and is necessary because the phase of subcarrier (from which the clocks are derived) relative to horizontal syncs is arbitrary and undefined. The principle of operation is to take as the start of the line the first edge of subcarrier after the expiration of a time t_1 or t_2 starting from the horizontal sync.

The subcarrier edge is made to alternate from positive to negative going on adjacent lines so that all lines in the field start at the same horizontal position. The difference between t_1 and t_2 is arranged to be half a cycle of subcarrier frequency. If, say, t_1 is in use at a particular time, it will continue in use until such time as the subcarrier edge falls within a predetermined window centred on the expiration of interval t_1. At this point, the circuit switches over to using t_2. In this way, hysteresis is introduced so that there is never a situation of indecision as to which clock is to be used for the first picture point.

The time t_1 or t_2 is the sum of the pulse width of monostable BF and the delay caused by R3 and C5, the output of CF pin six causing the change between t_1 and t_2 via R14 (VR1 should be adjusted so that the pulse width at BF pin twelve changes from 5.8μs to 5.94μs (approximately) as the subcarrier phase of the video input is varied). The subcarrier (WFSC) entering on A13 is inverted on alternate lines by the action of the signal from BE pin six, at BE pin three, and the result is synchronised in phase with W4FSC at CF pin nine. The first rising edge at this point after the time interval t_1 or t_2 (that is after EE pin eleven has gone high) causes CE pin five to go high; this signal is the bit picker output and defines the start of the active line. The pulse generated at EE pin three is set by R4 and C70 to be twice as long as the delay caused by R3 and C5. Thus, the positive edge at EE pin eleven is in the middle of the pulse at EE pin three. If the subcarrier edge at the clocks to CE occurs within the time of this pulse (which defines the window referred to earlier), the output of CE pin nine will cause CF pin six to change state, thus changing from t_1 to t_2 or vice-versa.

The bit picker output (CE pin five) clocks FH pin five high, which enables counter EH, EF to count. After the correct number for clocks, as decoded in BA, FH pin five is cleared, thus stopping the counter. Hence this signal is the horizontal blanking signals required in colour (i.e. $\overline{\text{MONO}}$) mode for gating the clocks, etc.

(b) Video Data Path

The digitised data from the ADC passes through ROM BD, which acts so as to limit the possible range of values representing normal video, and may be enabled onto the input of the editorial store by CD.

Luminance and Chrominance components of data on the system bus (originating at the disc or border generator) are registered into DC and DA respectively by the Interpolated Disc Picture Point Clock signal (IDPPCK) on B44. The chrominance is modulated onto a disc rate subcarrier signal from BE pin eight (whose generation is described below) by the action of EB and EA. The luminance and modulated chrominance components are then added together

in FA, FB and GB, whose output is limited should overflow or underflow have occured, by FC and GC.

The output here is registered into DD by IDPPCK, whose output may be enabled onto the input of the editorial store. If a border is being written into the editorial store (as indicated by a high at FE pin nine), it is necessary for correct operation of the key mechanism to ensure that the value 255 (all bits high) is not written. Hence the occurance of this level at the output of the adder is detected by HB, which causes the select input of the limiter to go high. However, as the signal at FE pin nine is fed into the LSB at FC pin three, this will cause limiting to occur at 254, rather than 255 in the case of video.

The disc rate subcarrier signal used by the encoder is made by dividing IDPPCK by four in HH. During the transfer of a picture from the disc to the editorial store, data selector GH is set to select its B inputs, because the address decoders AA and CA are not activated; hence both halves of HH will be preset by each Interpolated Disc Line Clock (IDLCK) at A44, and the signal at HH pin eight will start in the same phase on each line. The two halves of GH are cleared at the beginning of each picture transfer by Disc Clear (DCL) at B45, and divide IDLCK, by two and by four. The output of the appropriate half is selected in FG, according to whether the picture is a field or frame mode picture, (as registered into DB pin twelve by the computer), to alternate the phase of the signal at BE pin twelve line by line or on alternate pairs of lines respectively. The phase of the resulting signal is further alternated by the Disc Field Bit (DFB) at A45, giving the required disc rate subcarrier signal at BE pin eight.

The key input to the machine enters the card on A39, and its level is compared with the voltage at the slider of VR2 in comparator GA. The output of GA is thus a TTL key signal. VR2 should be set to slice the input key most reliably, or to its maximum negative excursion if the key input is not being used. The TTL key signal is synchronised with W4FSC in BG, and suitably combined with the signal at EC pin ten (derived from the computer command registered into DB by address decoder AA) to enable the correct data onto the editorial store input: Disc mode, enable DD; video mode and key high, enable CD; video mode and key low, enable DE which gives the KEY level of 255 (all bits high).

(c) Border/Matte

To write a border or matte into any of the frame stores, the computer first loads the required luminance, (B-Y) and (R-Y) values into registers BC, BB and AB via the system bus under the control of address decoders AA and CA. Next, it presets the phase of disc rate subcarrier as appropriate by switching data selector HG to select its A inputs, which are part of the system bus. Note that for Border/Matte write, this presetting is calculated for each individual line by the computer.

Hence FG pin four is held low by the disable signal at pin fifteen so that the setting of GH does not affect the phase of the disc rate subcarrier generated.

Then, via a negative going pulse at CA pin ten, it loads into counter HD, GD, FD the number of picture points required, the rising edge of the pulse generated at HE pin twelve actually clocking this number from the system bus into the counter. The pulse generated at HE pin four simultaneously presets FE pin five high, thus disabling the counter. Also FE pin nine is clocked high, which holds the Req B line (B47) low (indicating to the computer that it must now wait for further access to the system bus) and illuminates LED1. The clock for the border counter is simply W4FSC divided by fourteen in GE. The first clock pulse at GE pin eleven after the preset to FE pin four has gone high clocks FE pin five low. This enables the counter and also enables clock pulses to pass through to GF pin eleven. The counter counts down to zero, at which point the carry out of FD pin fifteen prevents further clocks from reaching EE pin six and clears FE pin nine. In this way, the exact number of clock pulses specified by the computer reach GF pin eleven, from where they are enabled onto the IDPPCK line (B44) via part of buffer AE, which is controlled by decoding various outputs of the computer command held in register DB. As the computer cannot access the system bus whilst FE pin nine is high a 'panic' detect circuit is incorporated to prevent an irreversible system hang from occuring. In such a sutuation, the computer can abort the operation of the border/matte generator by setting the CSR mode to fifteen (all bits high) and setting TX/RX low. This is detected by BA and part of GF, and clears FE pin nine.

INPUT PROCESSOR CARD

17346

1. Circuit Description

The video at the input splits into two paths. In the first path, its passes through a low pass filter and onto a sync separator circuit. The syncs thus produced are used to phase-lock an oscillator at W4FH (a frequency close to four times subcarrier). From these clocks various clamp and input timing signals are produced; they also clock the ADC etc., in monochrome mode. In the second path, the video is clamped during back porch and buffered. Again the path splits into two. The first passes through an anti-aliasing filter, a remote gain stage and on to the ADC whilst in the second, the comonents in the subcarrier frequency band are extracted in a band pass filter and used to drive R-Y and B-Y demodulators. The R-Y demodulator drives the burst locked oscillator (BL0), which runs at four times subcarrier frequency to provide the lcoks for the ADC etc., in colour mode.

Composite video is input via pin AB11 and passes both the sync separator through R3 and to the input buffer and d.c. restoration loop through C2. In following the path to the ysnc spearator, the video is first buffered by AG, then low pass filtered by C21, L7, C22 and L8 to remove most of the chrominance components before being inverted by IE and buffered by TR6. From here is is applied to the sync separator consisting of HE, IE, JE and associated components.

In the sync separator inverted liminance is applied simultaneously to pin three of HE, pin three of IE and pin two (via R37) of IF. IE is gated on by TR7 at sync tip time. The sampled voltage is stored on C24 and buffered by JE before being applied to R41. HE is gated on at back porch by transistor TR8 with the resulting current store by C26 and buffered by JE, then applied to R42. The two voltages are summed at the junction of R41 and R42. and the resulting output is a d.c. level equal to 50% of sync tip amplitude. This is used as a reference by comparator IF which slices the syncs from the luminance applied to pin two. D2, D5, R32 and R33 are used for start-up of the sync separator. It has a composite sunc output at TTL level from pin four. This output is routed to pins three and four of JG, pin twelve and thriteen of JH and pin one of HH. It is also applied to the field separator consisting of TR9 and associated components which will be discussed later. JG is a 2h eliminator that feeds both JH and HH. THe Q output, pin four of HH is fed back to the base of TR7 to gate the sync separator input circuitry that samples sync tips. The Q output, pin thirteen of HH drives HG ans HH. HG pin twelve poutput the write line drive (WLD) signal whose period is determined by VR3, the picture phase adjust control. The Q output, pin five of HG triggers HG which in turn gates on FH for the H phase - locked loop circuitry via TR10. JH and HH generate a clamp pulse which is fed back to TR8 to gate the sync separator input circuitry that samples back porch, as well as to TR5 and HF.

The field separator, as previously mentioned, is driven by composite sync from IF. R44 and R44 level shift the TTL signal down and TR9 inverts it. R46 abd C28 integrate this waveform such that broad pulses trigger HG which generates clear write drives (CLWD) that are fed off the card via pin A39.

The other path for input composite video is that through C2 and on to the input amplifier and buffer consiting of BG, TR1, TR2, TR3 and TR4. VC1 allows some adjustment of the high frequency response of this stage before diring the input low pass filter, chrominance bandpass filter and d.c. restoration filter.

The d.c. restoration filter consists of C9, C4, L1 and C11 and is low pass to remove most of the chrominance, and high frequency components of the video. The resultant signal is applied to pin three of CH which is gated on at back porch by TR5. The resulting current is stored on C10 and the potential buffered by BH whose output is used to add a d.c. offset to the signal fed into the input amplifier threreby causing the signal to be clamped at a precise d.c. level at back porch time.

The chrominance bandpass filter consists of L9, C50, C52, C53, L6, L5 and C57 and is emitter folloed by TR11 before feeding the primary of T1 via C59. FC and GA are doubly balanced demodulated which form B-Y and R-Y quadrature demodulators. The deomodulated R-Y signal is connected via FB which buffers the signal to pin three of EB. VR2 is used to balance the output of FB at TP10. EB is gated on during burst time by HF triggered off back porch and the resulting current stored on C46 whose potential is buffered by FB. FB feeds FB and associated components which invert this error voltage as well as providing damping via C44 and R65. TP11 thus has a d.c. voltage proportional to the phase error between the burst locked oscillator (BL0) EA and incoming burst. This voltage is applied to the srystal controlled phase locked loop whic is running at 4FSC, to slew it into lock. One output of the BL0, pin seven, is connected to DA and DA which divide this 14.3MHz signal down by four to provide a 3.58MHz sugnal. This signal leaves th card from pin A45 as WFSC and can be chosen to be in any one of the four quadratures by links on DB. One quadrature is phase shifted by the combination of DC adn DC and applied back to the B-Y and R-Y demodulators via ED and ED. The phase shift introduced by DC and DC allows for remote control of hue by a signal input through pin A35. The other BL0 output pin eight is sent as an input to multiplexer DD which will be discussed later.

The demodulated B-Y signal is fed to FB and on through to HA. HA is gated on at burst time with the resultant current stored on C47 and the potential buffered by JE which also inverts the signal to drive the MONO transistor TR20 into saturation whenever there is a monochrome signal detected; VR1 has the effect of adjusting the monochrome detection threshold. This MONO signal controls DD and is fed out of the card via pin A36, and in mono form after inversion by DE via pin B37.

The purpose of the horizontal phase locked loop circuit is twofold. It is used to generate the H-locked clock and also the horizontal reset pulses necessary for the timing of the system. In the latter case the 14.3MHz output, pin seven from the line locked oscillator (HL0) DH is used to clock counters DF, EF and FF which together with PROM EG and locath DG divide down the 14.3MHz signal to provide the reset pulses. The write picture gate (WPG) output is fed to FH where it acts as a phase detector. The resultant error produced by gating of FH is buffered by EH and applied to the crystal oscillator to slew it into lock with incoming H. The ohter use of the HL0 clock is as the second input to the multiplexer DD. The output of DD provides clocks for the ADC, data latch AA and out of the card via pin A46 as W4FSC. The output of DD is chosen to be either the BL0 clocks or the HL0 clocks dependent upon the MONO signal.

In addition, the HL0 output is divided down by EE and EE to generate a write colour phase ident (WCPI) signal which leaves the card on pin A40.

The only other part of the circuit left to describe is that of the main video signal through to the ADC. Clamped composite vide is applied via R19 to 5MHz low pass filter. This is an anti-aliasing filter used to attenuate any high frequency components above 5MHz. The low pass filtered video is applied to pin twelve of CC which is a four quadrant multiplier that allows gain to be remotely controlled. VR4 allows the nominal gain of CC to be set and VR6 any input offset to be balanced out. The output of CC is applied differenitally to CB. TR15 and TR17 allows extra current to be fed into current buffers TR12 and TR13 in a manner controlled by VR7 so as to affect black level of the video signal. Set up can be remotely controlled by a signal through pin A13. CB, together with TR14, drives the ADC. At pin three of CB a d.c. voltage is summed in to add to the DC on which the video is sat. This voltage is derived from the –2V reference which also feeds the ADC. The reference is supplied by CA from D10 and the voltage can be finely adjusted by VR5. The video is converted to an 8-bit word word updated at a 14.3MHz rate and sent to the data latch AA, the data being output throught pins B51 and B58. Sliced video is avialable at pin B21.

EXHIBIT 8

MCI/QUANTEL

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NEWS

MARCH 1, 1980

The DLS 6000 Digital Library System - A Preliminary Description

Introduction

The revolutionary Quantel DLS 6000 Digital Library System represents a new generation of still stores. The system permits not only significant improvements in basic performance over existing techniques, but also allows several unique capabilities to be included that make the unit a complete production tool.

Also included is a novel off-line storage technique that permits a virtually unlimited library. (The off-line system will not be described in this paper but can be seen at the NAB in Las Vegas.)

The Basic Philosophy

The idea of storing television stills on a computer disc in digital form rather than as conventional 35mm slides is not new. The advantages of this approach include high integrity of information, very simple generation of stills, ease of program compilation with greater immediacy, lower running and maintenance costs, better security, and easier management of a central library.

However, existing equipment is bulky and has no production facilities to allow simple integration of stills into a program with the flexibility increasingly being demanded by production staff.

The Quantel DLS 6000 transcends both these obstacles, achieving small size through high packing density on disc, and offering all the production facilities required by the modern program maker.

The philosophy behind the DLS 6000 is the marriage of solid state framestore techniques with standard computer disc technology. The use of completely unmodified computer disc systems gives high reliability and low cost -- particularly important if the machine is to be readily adopted by the broadcast industry, and critical if the unit is to be used in outside broadcast vans.

The disc technology used is the IBM-developed Winchester system. This is the latest very high density, low cost disc system now adopted as standard by the computer industry and available from several manufacturers. Capacities of up to 160 M bits are possible in units less than 8 inches tall.

However, if standard computer disc systems are used, some way has to be found to overcome the fact that typical data rates on disc are only 8 M bits/sec as opposed to greater than 100 M bits/sec for real time digital television. The solution lies in the provision of solid state framestores used as buffers before and after the disc.

The computer disc-based still store then essentially comprises the disc itself and a solid state framestore able to operate at both real time video rates and disc rates. Recording is achieved by capturing the picture at real time and then writing it to disc more slowly. Replay is gained by the same process in reverse, the information being transferred from disc to the framestore at 8 M bits/sec and then displayed to the outside world at full video rate.

Although only a single framestore and the disc are required, considerable improvements can be made to the ease with which the machine can be used if more than one framestore is included. The DLS 6000 contains three.

The basic task of the system is to replay the correct picture from the disc store. However, the usefulness of the system can be greatly enhanced if, at the same time, the size and position of the replayed picture can be defined in accordance with the requirements of the rest of the production.

Special circuits in the DLS 6000 allow this function to be available for multiple images to allow montages to be produced. The addition of a multiple border facility completes the full production package.

Features of the DLS 6000

High Capacity

Up to 340 pictures can be stored on one disc drive and multiple disc operation is allowed giving, say, 3400 pictures randomly accessible from 10 discs. The number of disc drives allowed is unlimited, but most users requiring very large library storage will make use of a novel off-line back-up store.

Small Size

The high capacity of the DLS 6000 does not preclude its use in outside broadcast vans since the device is remarkably small - just 7" for the disc unit and 10½" for the DLS 6000 unit itself.

High Fidelity

The Quantel tradition of high fidelity is maintained in the quality of the images of the DLS 6000 at all times whether modified in size

or not. At all sizes and shapes the unit displays virtually transparent image quality.

High Change Rate

Pictures can be changed at a rate of two per second with complete random access; thus, no cache memory of the day's program requirement has to be prepared.

On-Air Picture Change

Although the change rate is limited to two per second, the additional framestore circuitry in the DLS 6000 allows vertical interval switching between pictures. Thus, the switch is instantaneous.

On-Air Transitions

A mix/effect bus can be eliminated by utilizing the digital transitions available in the DLS 6000. Changes between one picture and the next can be by means of a simple cut, a programmable dissolve, or even a wipe.

Picture Reposition

The output picture of the DLS 6000 can be repositioned by the technical director at will.

Picture Compression

The DLS 6000 will reproduce the stored image at any size from normal (full size) down to virtually zero size. This feature, together with the reposition system, allows the technical director to define the exact size and position of the reproduced still to suit his production without resorting to any other digital effects device.

Picture Enlargement

The image can be enlarged up to two times to allow selection of a chosen portion of a still.

Variable Aspect Ratio

The aspect ratio of the image can be varied away from the standard 4 x 3 to any rectangular shape.

Multiple Picture Handling

The DLS 6000 is capable of reproducing as many pictures as are wanted at the same time. This capability is clearly an adjunct to those of compression and repositioning and is used either to show at the same time a number of participants in a discussion or event, or even to build up a complete montage of images. The pictures can be recalled

from disc one at a time to show the viewer the build up, or simultaneously so that only the finished composite is seen.

The Borders

The DLS 6000 includes its own border generator capable of changes in hue, saturation, luminance and width. This is applicable to all pictures being shown, although different images can have quite different border parameters at the same time.

The border generator also includes a background or matte generator, further releasing the switcher for other functions.

Multiple Outputs

Three outputs are available with the DLS 6000, two program and one preview. Internally generated transitions are possible with both program outputs or they can be used together to utilize more exotic wipes in a switcher. The DLS 6000 generates keys that match the pictures at all times.

Preview

The DLS 6000 has its own preview output which can be operated without effecting the on-air program or transitions. The preview allows the varying size or position of images to be chosen by means of cross-wire cursors controlled by joysticks. It also contains a unique feature for fast viewing called "BROWSE".

"BROWSE"

"BROWSE" provides the ability to look through the contents of the disc by displaying 25 images at one time and slowly moving them down the screen. This rolling list of pictures allows easy viewing to find the desired frame or alternatively permits the showing of pre-chosen slides waiting in the 'stack' for display on a program.

On-Air Editing

On-air display or transition is unaffected by preview contents; similarly the unit allows the capture and recording of incoming material during on-air display or transitions. This feature is essential if the unit is to be used to its fullest extent in the news studio.

Asynchronous Operation

The input of the DLS 6000 can handle asynchronous information to allow stills to be captured from incoming ENG material.

Graphics Handling

The DLS 6000 is capable of keying stored graphics over displayed images, releasing the switcher from this function. Graphics may have their size

and position defined independently of picture information; in this way, perfect readability is assured for all sizes of titled images.

Digital Re-recording of Composite Pictures

Composite pictures created on the preview monitor can either be stored as control parameters to ensure recall on demand on the program outputs, or they can be re-recorded back onto disc as a complete new picture at an individual location.

Editing System

Complete sequences of commands to the DLS 6000 can be set up and stored to allow simple single-button operation during program time. The editing system does, however, allow simple addition or deletion of items to ensure ease of operation in a fast-moving news broadcast.

The inclusion of a DEC LSI-11 minicomputer as the host processor for the system allows the simple addition of standard computer peripherals at a later date to accomodate even more powerful editing systems.

Control Delegation

The control of the DLS 6000 can be timeshared between several stations including, during a live broadcast, separate preparation and replay panels. This permits the technical director to remain divorced from the choice of stills created from incoming ENG material.

Future Expansion

As with all Quantel products, the DLS 6000 has been designed to allow future expansion by the retrofitting of options. The first of these is likely to be an increase in storage capacity allowing up to 700 pictures per disc drive.

The System

The previous section defines the DLS 6000 as requiring an input store to capture video information, two program output stores for displaying the output, and one preview output store to permit viewing of disc information without interference with program output. These facilities readily define the block diagram of the system, as shown in Figure 1.

The recording chain is shown at the top of Figure 1. Input video enters the system and is immediately converted into digital format and passed to a framestore at full video data rate. This input framestore acts as a freeze frame device and allows the user to select still pictures from the incoming live video. For convenience, the link from the output of this store to the preview output from the DLS 6000 has not been shown, but in reality the video follows this path allowing the user to observe the incoming picture at all times, whether live or frozen.

Once the chosen image has been frozen in the framestore it is read out

from the store at disc data rate via a data processor section to further reduce data rates, and then via the disc formatter to block the information suitable for writing on to the disc.

The disc itself is a latest generation sealed Winchester-type drive with high packing density. The heads are of the flying type but the construction of the disc eliminates the need to have expensive and unreliable head retraction mechanism; the heads actually land on the disc surface when the platter is not in motion. The disc data rate allows a picture to be generated in 0.5 seconds. The total package is highly reliable and rugged, and includes parity check circuitry for optimum data integrity.

The replay chain, shown at the bottom of Figure 1, is obviously more complex than record due to the increased number of framestores and program output facilities. Data from the disc passes through a disc re-formatter where the information is sorted out from its blocks and then onto the data processor where it is unpacked. The information is passed to one of the three framestores and it is at this point the size change mechanism operates. If the information is routed via the preview store then no other processing is done other than reading it out of the store at full video rate into a DAC and onto the display via a proc amp. If the data is fed to one of the program stores then it is subsequently passed to a digital combiner assembly that performs the appropriate wipe, cut, or dissolve functions. Also the combiner copes with the addition of borders or the keying of caption information over pictures or colored matte.

For convenience one framestore is shared between the video input facility and the preview output. Not shown in Figure 1 is the host DEC LSI-11 mini-computer that controls the whole machine and is responsible for all housekeeping tasks, the operation of the control panel, and the editing system.

The Control System

The philosophy behind the control system for the DLS 6000 is based on the concept of Pictures, Slides and Groups.

A picture is defined as an image on disc with a number allocated to it at the time of recording. A picture is normally recorded on disc at full size to give maximum flexibility on replay.

A slide is a picture on replay that has the parameters of size, postion, transition type, time, etc. allocated to it. The number of a slide need not be the same as the number of the picture that the slide depicts.

A group is a collection of up to ten slides.

The importance of these three definitions will become clear when the display system and control panel are described, but the important thing to remember is that, with this machine, defining a picture merely by a number is insufficient due to the extra facilities available. Therefore, both the picture and what is to be done with it must be defined before

displaying on the program output.

The Computer Display

The extra degrees of freedom made available by the DLS 6000 production features makes it necessary that, at both the preparation time and the program time, the operator always has a clear picture of exact machine status.

In order to give the user this clear indication of the situation, a video display system has been added to the host computer. It is via this display system that all setting of parameters is achieved.

The computer display output is added to the preview output and shares the preview screen.

There are three types of computer display available to the user Edit, Ident and Menu. A cursor display is added to all these to allow the size and shape of images to be defined.

The Cursor

Four lines on the preview monitor define the top, bottom, and two sides of the picture. Whatever size, position and shape is enclosed by the four lines is filled by the picture called from the disc.

In the case of expansion, the area inside the cursors defines the portion of the original picture (taken as full screen) that will be displayed.

The cursor is not available on the program outputs.

The Edit Display

A typical example of the Edit Display is shown in Figure 2. Note that the slide number is independent of the picture number, as described earlier. Size and position parameters are set with the joysticks on the control panel; the legend on the display merely reminds the user of the particular condition set.

Border has to be defined as on or off. If on, then again the parameters are set from the control panel.

Transitions between one slide and the next can be defined as dissolves, cuts, wipes, or supers. In the case of supers, slides are super-imposed on one another to create montages of images.

Transition times are defined under the cue headings. Normally, the advance from one slide to the next has to be initiated by the start button or the control panel; unused locations are skipped. Instant headings are usually used with super-imposed pictures but alternatively, the 'start' initialization can be used in which case the montage is built up before the viewers' eyes.

'Ext' denotes that the system should wait for an external cue from another device such as a computer editor.

Locations on the display that do not have any entries are 'DON'T CARE' cases. In these circumstances, the computer will define the last parameter taken. In this way, if at the beginning of a Group, size and position are defined but all other slides leave this column blank, then all subsequent pictures will be displayed at the same size and position.

The Ident Display

The "BROWSE" mode for the DLS 6000 allows the user to look through the contents of the disc 25 pictures at a time on the preview monitor. The 25 pictures move slowly down the screen with new rows of 5 being added as the first 5 fall off the bottom of the screen. This feature gives the viewer the electronic replacement for holding a 35 mm slide carrier up to the light.

The ident display overlays the true picture number on the "BROWSE" display so that the various chosen pictures may be easily identified.

The Menu Display

The Menu display is a special option that allows selection of modes of use of the machine.

The Control Panel

Figure 3 shows the control panel for the DLS 6000, which occupies 8" x 4" of panel space.

The long rectangular area towards the top of the panel is an alpha-numeric display that is used by the machine to indicate its status and allow a degree of conversation with the user.

The joysticks at the top right are used to change the size, shape, and position of the displayed image and the keypad underneath is the means by which numbers are assigned to pictures, slides, or groups, and through which all parameters are entered into the machine.

The 'clear' button cancels the action of the joysticks, ensuring that the image is normal size and position.

FREEZE is self explanatory except that it should be remembered that this results in an image being frozen in the input store and not transferred to the disc. Transfer is achieved with the RECORD button into a picture location defined by a keypad number. The FRAME/FIELD button decides whether the picture is transferred at frame or field resolution. ERASE removes a picture from disc, again defined by keypad numbers.

GROUP, START, and STOP are associated with the editing system and control couplings of pictures that can be called up, not by their real

numbers which may be scattered over large areas, but by simple order in a sequence. This will be described more fully later.

The two buttons △ and ▽ move a cursor arrow up and down the computer display to select various functions.

SELECT controls which of the various possible types of computer display is being used, and CHANGE operates on some of the heading of the computer display to change options in sequence.

PICTURE is used to denote a demand for a location on disc to be accessed.

Across the top of the panel are four toggle switches used to control the parameters of borders or matte.

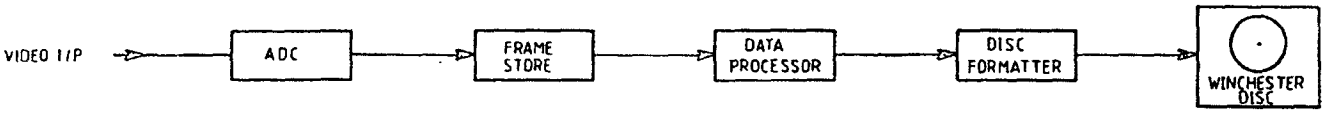
Timesharing Use

The DLS 6000 is designed to be capable of single or two-person operation; thus two control panels may access the machine simultaneously.

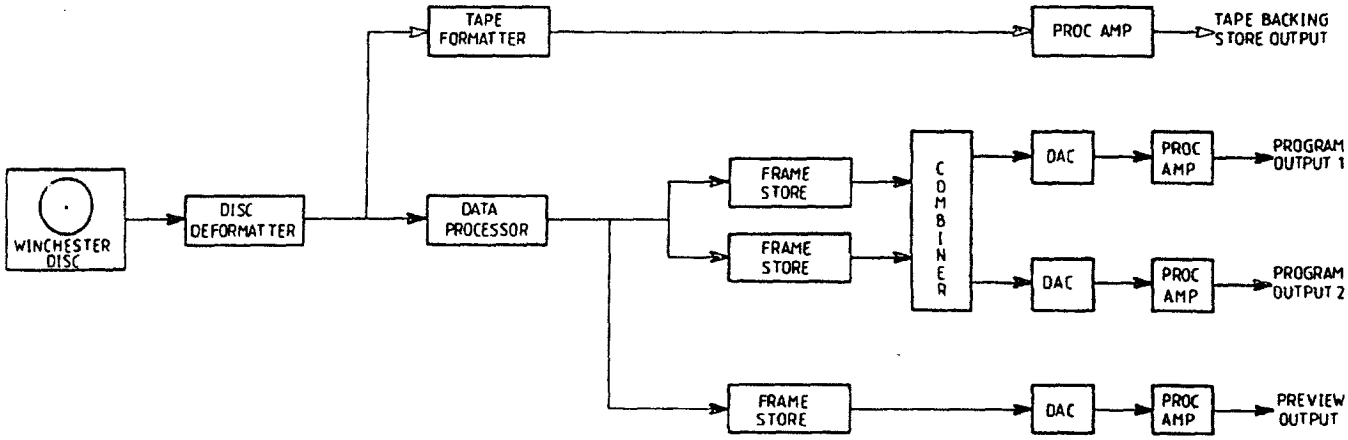
The best way of describing this function is a typical long news program in which the pictures for the end of the show have not been decided upon prior to air time. In these circumstances, the technical director will have a control panel in front of him associated with the switcher, while a production assistant or 'composer' will also have a control panel. Both are identical, but one is used virtually always for replay (the TD) and the other for record (the 'composer').

The TD will merely move from slide to slide within a group without necessarily worrying about choosing the content of the slide. A Group will be assigned to a particular story or item in the newscast. If the content of the story changes, then the 'composer' will modify the pictures accordingly; if stories are inserted or deleted as the program develops, then the TD merely has to be told which is the group containing the story being covered. At all times the 'composer' can be busy building the material while the program outputs of the machine are on-air.

The timesharing system also allows the disc system to be switched from studio to studio if desired.



THE RECORDING CHAIN



THE REPLAY CHAIN.

FIGURE 1. BLOCK DIAGRAM OF THE DLS 6000.

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GROUP 123

SLIDE	PICTURE	SIZE & POSITION	BORDER	TRANSITION	CUE
0	23	NORMAL	ON	DISSOLVE	20
1	18	COMPRESS	OFF	CUT	
2	14	ENLARGE		WIPE	10
3					
4	36	COMPRESS		SUPER	INSTANT
5	100	COMPRESS		SUPER	
6	23	COMPRESS		CUT	
7					
8	11	NORMAL		CUT	EXT
9	10				

NEXT GROUP 138

FIGURE 2. TYPICAL EDIT DISPLAY FOR DLS 6000

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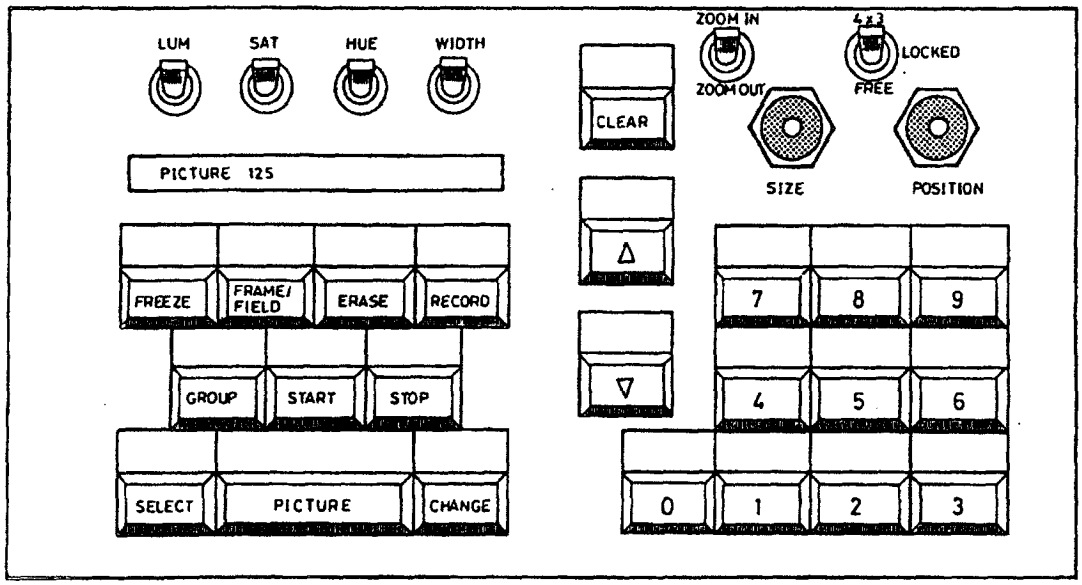

FIGURE 3. DLS 6000 CONTROL PANEL.

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